Altera hurdles 90-nanometer challenges

By Margarette Teodosio

Industry change is never easy. Either you adapt, or stay put and be left behind. With guaranteed huge earnings from the ASIC market, Altera Corp. did the former and came up with its Stratix II and Cyclone II families of FPGAs.

However, as with all kinds of change, it was not smooth sailing all the way. The transition to the 90nm mode has certainly not been easy, the company admitted, it has required more in-depth analysis, research and testing than prior nodes.

Before jumping over the 90nm fence, Altera collaborated with its foundry partner Taiwan Semiconductor Manufacturing Co. Ltd to address and resolve the 90nm and low-k challenges before entering production. As they developed and ran multiple test chips, they encountered three key challenges: interconnect, power management and design manufacturability.

Ben Lee, VP for Asia-Pacific at Altera, said that they chose low-k to address the interconnect issue. "We decided early on that for 90nm to be successful, we have to use a mainstream process at TSMC," he said. "The reason why you want to use a mainstream process is because you can drive the yields up and the defects down quickly with volume."

The second issue that needed to be addressed was power management. "When going to 90nm, there's a lot of leakage current because of the transistors, as they are so small and there are a lot of process-induced effects," said Lee. To overcome this, they had to design for 90nm. "We had to re-architect the chip to fully take advantage of 90nm and design for power."

Lee added that engineers cannot just simply take a 0.13µm or 0.15µm design and quickly shrink it to 90nm. "It would be a disaster in terms of power," he exclaimed.

Altera and TSMC conducted a lot of tests on whether they would use double oxide or triple oxide based on performance and cost. Altera finally settled on the double-oxide process for all its 90nm projects. As they hoped and expected, it turned out to be a standard for 90nm.

The third challenge was design for manufacturability. "Design for manufacturability is not something where you just think about it before the design and then try to work for it after the exact design is done."

Altera had their engineers check for process limitations throughout every phase of the design cycle and made adjustments to every design stage to ensure enough design margins for the limitations. "It's one thing to design a chip and say 'we have this solution,' but it is another thing to be able to shift in volume," Lee said.

Additionally, Altera developed a new logic structure called adaptive logic modules (ALMs) for its Stratix II to increase performance without consuming unnecessary power.

The company claims that ALM addresses the growing usage of adder functions in FPGA designs, such as in wireless technology and DSPs. "ALM gives you a variable number of inputs to choose from so you can maximize the use of the logic and the silicon," Lee said.

At present, Altera is also focusing on its HardCopy devices, which are touted to be the industry's first structured ASICs that offer a good alternative to traditional ASICs. According to the company, the power consumption of these devices is on average 40 percent lower than the corresponding FPGA.

Commenting on other key players in the industry, Lee said, "Our competitors are about one year behind on 90nm and high-density FPGAs." He added that Altera has been doing for years what the other manufacturers say they are doing now in terms of modular blocks in FPGAs. □

Smallest transceiver saves big in power

By Rey Buan Jr.

Power consumption efforts in the communications arena may undergo significant improvements with the introduction of what appears to be the smallest transceiver in the market. Developed and released recently by Xignal Technologies AG, the XT38720 is a 10Gbps CMOS XFI transceiver that currently has the smallest active footprint area of 4mm^2 and expends ultra low-power consumption of only 350mW. With its size and power advantages, the new XFI-compliant transceiver helps trim down cost and improve data transmission performance in local-, metro- and wide-area networks.

The Munich-based IP solutions provider developed the XT38720 using 0.13µm CMOS process technology and has an on-chip clean-up PLL that only needs a simple external RC filter to be connected to the device. The transceiver also has a selectable pre-emphasis that ensures optimum signal integrity over FR4 grade PCB material and is suitable for data rates from 9.95Gbps to 10.7Gbps.

Xignal's ability to provide devices in 0.13µm CMOS process–that normally requires bipolar, if not GaAs or SiGe–has been doing great things for them for the past years. With current issues surrounding the shrinking process, Holger Hoeltke, VP for marketing at Xignal, is positive that the 130nm-vs.-90nm process debate will not have any significant effect on Xignal's product development.

"Analog design doesn't really benefit from the shrinking process," said Hoeltke. "Xignal has been keen in using 0.13µm CMOS process technology to almost all of its products because it addresses certain markets such as the multigigabit copper link segment. And in this market, the gate length of CMOS at 0.13µm becomes pretty handy."

Hoeltke: Analog doesn't benefit in the shrinking process.

Moreover, it is difficult to fold the shrinking process in analog design. Better frequency comes from smaller gate sizes. However, the difficulty arises not from the shorter gate length, nor from the entire density, but on the leakage current that comes from the lower supply voltage that is imposed to the SNR.

"There may be a need for analog in even smaller feature size process technology. Designers should be prepared as designs become more difficult, and system providers should rethink about the partitioning of systems," Hoeltke said.

With its size, power saving feature and CMOS nature, the XT38720 can be integrated in SoC environments appropriate for 10Gbps over copper connections, 10Gb Ethernet and 10Gb Fibre Channel applications.

The XT38720 has the ability to serialize and deserialize 32 input-data streams to a single output-data stream, and vice versa. The high-speed serial I/Os are compliant to the XFI defined in the 10Gb Small Form Pluggable (XFP) module specifications. Having an integrated limiting amplifier, the product can also be used as a standard serial 10Gbps fiber optic interface with the help of a signal conditioner IC.

"Reducing the device's size definitely reduces cost," said Hoeltke. "Moreover, going to small modules means you have to have low power ICs. Since the XT38720 consumes low power, it significantly reduces design constraints and thus increases the device's port density."

As mobile communication devices continue to evolve, more high-speed broadband systems will need high-performance devices that help minimize chip-to-chip interface issues. Moreover, these demands would continue to require additional power requirements on the overall system that could potentially cause an increase in the device size. □

Storage firm BitMicro acquires patent

By Kathryn Gerardino

Solid-state storage company BitMicro Networks Inc. recently acquired a patent, which it claims to eliminate functional deficiencies in storage devices by testing I/O functionality during a storage operation.

As capacity in storage devices increase, it becomes increasingly difficult to perform I/O functions such as write, read and erase. With the new patent called "Method and Apparatus for Testing a Storage Device," such functional deficiencies can be avoided. This innovation is the core technology found in the E-Disk Analyzer of BitMicro's proprietary flash analysis development system.

Testing a storage device may include repeatedly reading and writing test data across selected or all memory locations available on the drive. Erase operations may also be performed. The test data and its address must be accounted for so that data subsequently read at the same address may be verified.

Data verification and I/O functionality testing become increasingly difficult to accomplish since it becomes hard to distinguish between similar test data that were written at adjacent locations at different time intervals. Increasing the different types of test may reduce confusion between data stored at adjacent addresses.

The E-Disk Analyzer is a dlash analysis development system that emulates and tests flash memory in a solid-state disk. It is a software tool that complements BitMicro's E-Disk product line.

The E-Disk product line is a drop-in replacement for standard rotating hard drives but the architecture behind the product is more complicated and calls for a more powerful testing tool, said Jhay Gregorios, the company's engineering manager.

Providing testing and reporting capabilities, E-Disk Analyzer is used by the company's hardware, manufacturing, firmware application and field engineers in all phases of the E-Disk flash drive's lifecycle. It is also a key to diagnosing even the most complex problems in laboratories and even in the field. Aside from being a critical component in the company's internal testing procedures, the E-Disk Analyzer also has versions for customers who opt to perform additional testing on their purchased products. □